REMARKS/ARGUMENTS

Claims 1-21 were pending. No claims have been amended, added or canceled. Hence, claims 1-21 remain pending.

The Office Action of 5/8/2006 rejects claims 1-5 and 9-21 under 35 U.S.C. 102(b) as being anticipated by Amick (U.S. Patent No. 6,650,157). Further, the Office Action of 5/4/2006 rejects claims 1-21 under 35 U.S.C. 102(e) as being anticipated by Masenas (U.S. Patent No. 6,525,615). Applicant respectfully traverses the rejection.

Claim 1 provides a clock synthesizer including, *inter alia*, a phase interpolator configured to introduce at least one phase of the source clock signal between a pair of phases and to successively output the phases to derive the output clock signal having a stepped up or stepped down frequency. Thus, in contrast to a PLL based clock synthesizer that provides a voltage feedback to a voltage controlled oscillator in order to increase or decrease a synthesized clock frequency, the invention as set forth in claim 1 inserts additional clock pulses into an output clock stream to increase clock frequency. An example of this is shown in Fig. 5a where Clk_{OUT} includes six positive clock pulses corresponding to the five positive clock pulses of phase P0 between times t1 and t6. Specification at p. 13, ll. 17-21 ("1 clock cycle is effectively inserted into the source clock over 12 source clock cycles to derive the output clock Clk_{OUT} with a stepped up frequency.")

The specification reinforces this distinction by teaching that "[c]onventional clock synthesizers . . . typically employ a Phase Locked Loop (PLL). However, PLL-based synthesizers have drawbacks in that they are relatively costly and bulky and typically consume a significant amount of power. These drawbacks can preclude the implementation of PLL-based clock synthesizers within low-cost low-power Integrated Circuits (ICs)." Specification at pp. 1-2. Thus, it would not be expected that a reference teaching conventional PLL techniques would disclose, teach or suggest the invention as set forth in claim 1.

As Applicant understands them, the cited art are merely forms of PLLs that were admitted in the background of the specification, and thus should not be expected to disclose, teach or suggest the invention as claimed. In particular, Masenas discloses a

"phase selector within a digitally controlled phase-locked loop". Masenas at Abstract. As with any phase-locked loop system, a control is provided to control frequency by providing a voltage or current feedback to a respective voltage controlled oscillator or a current controlled oscillator. Masenas at col. 5, ll. 11-17. As such, it is no surprise that Masenas fails to disclose, teach or suggest the insertion of additional clock pulses into an output clock to change frequency as set forth in claim 1. Hence, for at least the aforementioned reason, Applicant respectfully requests withdrawal of the rejections based on Masenas.

Somewhat similarly, Amick describes a delayed lock loop system that can "regenerate a copy of [an input] clock signal at a fixed phase shift from the original." Amick at col. 1, ll. 15-17. Such an approach provides a desired phase shift on a clock relative to some associated data. This helps alleviate problems associated with time delayed clock signals due to, for example, heavy loading and routing long distances. See e.g., Amick at col. 4, ll; col. 2, ll. 50-56. Amick does not, however, disclose teach or suggest insertion of additional clock pulses into an output clock to change frequency as set forth in claim 1. Hence, for at least the aforementioned reason, Applicant respectfully requests withdrawal of the rejections based on Amick.

As neither Amick nor Masenas discloses teaches or suggests each limitation of claim 1, Applicant respectfully asserts that claim 1 is allowable over the cited art. Further, as claims 2-11 properly depend from allowable claim 1, Applicant respectfully requests withdrawal of the rejections of the aforementioned claims and allowance thereof.

Claim 12 provides a method of operating a clock synthesizer that includes, *inter alia*, introducing at least one phase of a source clock signal between each of a pair of phases and successively outputting the phases of the source clock signal to derive the output clock signal having a stepped up or stepped down frequency by the phase interpolator. As set forth in relation to claim 1 above, none of the cited references disclose, teach or suggest such a limitation. Hence, Applicant respectfully requests withdrawal of the rejection and allowance of claim 12. Further, as claims 13-21 properly depend from allowable claim 12, Applicant respectfully requests withdrawal of the rejections of the aforementioned claims and allowance thereof.

CONCLUSION

In view of the foregoing, Applicant respectfully asserts that all claims now pending in the application are in condition for allowance. Hence, an early allowance of all such claims is earnestly requested.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees under 37 CFR 1.136, to the deposit account of the assignee, Texas Instruments Incorporated, Account No. 20-0668.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 720-266-4728.

Respectfully submitted,

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